FROM THE ORGANIZING COMMITTEE

We have a great pleasure to invite you to IEEE EAST-WEST DESIGN & TEST SYMPOSIUM – EWDTS’07!

The purpose of the symposium is to coordinate and exchange experiences between leading scientific schools and experts of the Eastern and Western Europe as well as of the USA in the field of digital systems design and testing.

From the one side, an overview of the state-of-the-art and of the most important progress trends of the industrial design and test will be presented by western researchers.

On the other side, an overview of achievements and research results obtained by the scientists of the post socialistic states during the last five years will be presented by the researchers from Eastern countries.

We are happy that EWDTS is becoming a world known as we have seen the interest of Eastern and Western European scientists in mutual collaboration. As a result of this collaboration we can see the penetration of new technologies to the market of Eastern Europe and to the university education. The feedback is determined by inputs of West-European scientists in research activities of Europe and USA.

We would like to thank: Yervant Zorian, Raimund Ubar, Andre Ivanov, Samvel Shoukourian (with the Armenian team), Zainalabedin Navabi (with the large Tehran team), Lyudmila Nesterenko, Vladimir Pavlov and Alexander Ryjov for taking an active part in organization of the conference, for financial, technical support, for international activity in Ukraine in the field of higher education, overall support of the university, support in preparation and holding of the symposium. The greatest appreciation to all official EWDTS’07 sponsors (Cadence, Echostar, Intel, INTSPEI, Mentor Graphics, National Instruments, Synopsys, Virage Logic) provided the best quality of financial support. We especially thank the Rector of Kharkov National University of Radio Electronics, Professor Mikhail Bondarenko, for overall support and active personal participation in preparation and holding of the symposium. Also we thank all contributors for high-level technical program and presentations.

Finally, we welcome all the participants of the EWDT'07 symposium and wish you successful discussions and a pleasant stay in Yerevan!

EWDTS'07 Organizing Committee
## ORGANIZING COMMITTEE

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<thead>
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<tr>
<td>V. Hahanov</td>
<td>General Chair, Ukraine</td>
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<tr>
<td>Y. Zorian</td>
<td>General Chair, USA</td>
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<tr>
<td>M. Karavay</td>
<td>General Vice-Chair, Russia</td>
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<td>R. Ubar</td>
<td>General Vice-Chair, Estonia</td>
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<tr>
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<td>Program Chair, Armenia</td>
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<td>D. Speranskiy</td>
<td>Program Chair, Russia</td>
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<td>M. Renovell</td>
<td>Program Vice-Chair, France</td>
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<td>Z. Navabi</td>
<td>Program Vice-Chair, Iran</td>
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<td>V. Saposhnikov</td>
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<td>Publicity Chair, France</td>
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<td>S. Mosin</td>
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<td>T. Atoyan</td>
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<td>S. Chumachenko</td>
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<td>O. Melnikova</td>
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<td>M. Kaminska</td>
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<td>K. Mostova</td>
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<td>V. Obrizan</td>
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## LOCAL ORGANIZING COMMITTEE (ARMENIA)

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<td>Ashot Avagyan</td>
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<td>Naira Nikoghosyan</td>
<td>Credence</td>
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<td>Arman Kuchukian</td>
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<td>Varoujhan Mahserejian</td>
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<td>Hrach Makaryan</td>
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<td>Gayane Markosyan</td>
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<td>Vazgen Melikyan</td>
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<td>Vahagn Poghosyan</td>
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<td>Samvel Shoukouryan</td>
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<td>Karen Vardanyan</td>
<td>UITE</td>
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<td>Bagrat Yengibaryan</td>
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<td>Avetik Yessayan</td>
<td>Virage Logic</td>
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REGISTRATION COMMITTEE

Maryna Kaminska  Kharkov Nat. U. of Radio Electronics, Ukraine
Homa Alemzadeh  U of Tehran, Iran
Avetik Yessayan  Virage Logic, Armenia

STEERING COMMITTEE

M. Bondarenko  Ukraine
V. Hahanov  Ukraine
Y. Shoukourian  Armenia
R. Ubar  Estonia
Y. Zorian  USA

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J. Abraham  USA
R. Bazylevych  Ukraine
A. Drozd  Ukraine
E. Evdokimov  Ukraine
A. Chaterjee  USA
E. Gramatova  Slovakia
S. Hellebrand  Germany
S. Hyduke  USA
A. Ivanov  Canada
V. Kharchenko  Ukraine
K. Kuchukjan  Armenia
V. Kureichik  Russia
A. Marchenko  Russia
A. Matrosova  Russia
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J. Skobtsov  Ukraine
The 5th IEEE East-West Design & Test Symposium is sponsored by the IEEE COMPUTER SOCIETY’S Test Technology Technical Council (TTTC).

The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members’ professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology.

TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters, and electronic broadcasts. All its activities are led by volunteer members. TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. You may enroll as TTTC member for 2007 (no dues or fees). To learn more about TTTC offerings and membership benefits, please visit: http://tab.computer.org/tttc

IEEE DESIGN & TEST OF COMPUTERS

IEEE D&T is a bimonthly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers, and researchers. D&T features peer-reviewed original work describing methods and
practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

– System Level Design and Test
– Embedded Test Technology
– Low Power Design
– Reconfigurable Systems
– Board and System Test
– Analog and Mixed Signal Design and Test
– System-on-Chip Design and IP Reuse
– Embedded Systems and Software
– Design and Verification/Validation

In addition, D&T publishes tutorial articles, perspectives, roundtable discussions, book reviews, viewpoints, conference reports, panel summaries, and standards updates contributed by authors working in the industry.

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– Jan/Feb: Biochips
– March/April: Advances in Functional Validation through Hybrid Techniques
– May/June: IR-Drop and Power Supply Noise Effects on Design and Test
– July/August: Special Section on CAD for Emerging Technologies
– Sep/Oct: Globally Asynchronous and Locally Synchronous Design and Test
– Nov/Dec: Design and Test of ICs for Secure Embedded Computing

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Tallinn University of Technology
Moscow Institute of Control Sciences
Kiev Institute of Modeling Problems in Power Engineering
RAS Institute of Design Problems in Microelectronics
GENERAL INFORMATION AND INQUIRIES

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E-mail: hahanov@kture.kharkov.ua
Internet: www.ewdtest.com/conf

BANKING

Generally, everywhere in Armenia you pay in Armenian drams (AMD). The currency units are: dram and luma. 1 AMD = 100 luma. The Armenian dram is a fully convertible currency internally in Armenia.

Foreign currency exchange facilities are available at major airports, railway stations, at large hotels, as well as in many private offices, called “Currency exchange”. Credit cards can be used in such places as banks and branch banks. Approximate currency exchange rate: 1 USD = 337 AMD, 1 EURO = 458 AMD.

CREDIT CARDS: Visa Card and Master Card are the most common cards. However, other cards are also accepted.

PROGRAM OF THE SYMPOSIUM

The program of the EWDTS’07 symposium will consist of oral presentations of contributed and invited papers, tutorial lectures, regular and short papers. The language of the conference is English, neither translation nor interpretation will be provided.

The time for oral presentations of regular papers is 15 minutes for presentation and discussion; short paper is 5 minutes.

WEATHER

September in Yerevan is generally sunny. The temperature can be typically 28 deg C during days. During nights, the temperature can drop to 18-22 deg C.
GENERAL INFORMATION

Total number of authors: 353.
Number of papers: 152.
Preliminary number of participants: 150.

Number of countries: 32 (Algeria, Armenia, Australia, Bangladesh, Brazil, Canada, Egypt, Estonia, France, Germany, Hong-Kong, India, Iran, Ireland, Italy, Jordan, Moldova, Nigeria, Norway, Pakistan, Poland, Romania, Russia, Saudi Arabia, Spain, Syria, Sweden, Taiwan, UK, Ukraine, USA).

KHARKIV NATIONAL UNIVERSITY OF RADIO ELECTRONICS

Kharkov National University of Radio Electronics (www.kture.kharkov.ua) was founded 77 years ago. It was the best University in USSR in 70th – 90th in the field of radio electronics. Today the University is the leader among all technical universities of Ukraine. Total number of students is more than 11000. The number of PhD and Doctoral students is more than 250. There are 650
teachers working for University. Among them there are 150 professors and 450 PhD. The laboratories of the University are equipped with more than 1100 computers.

Every year the University graduates more than 1832 bachelors, 1537 specialists, 184 masters. Graduate students of the University work in USA, Germany, England, Finland, France, Poland, Russia, Bulgaria.

The University has close contacts with universities from the following countries: Germany, USA, UK, France, Japan, China, Bulgaria, Finland, the Netherlands, Greece, Russia, Byelorussia, Czech Republic, Mexico, Serbia.

There are 50 contracts with the universities of other countries.

The University has obtained 67 grants during 2006/2007 years.

Scientific activity:

In 2006/2007 academic years 54 PhD theses and 12 doctoral theses were defended.

During 2004/2005 there were made more than 1000 publications. Among them are:

– 290 scientific articles;
– 550 thesis;
– 15 textbooks;
– 160 manuals.

The University publishes 5 periodicals. In 2006/2007 5 international conferences and workshops were organized by the University.

The University consists of 7 faculties. The faculty of Computer Engineering and Control is one of the best not only in the university but among other technical universities, which have similar specialties. During last ten years it has been taking an active part in scientific activities of state in the field of computer systems and nets design and application. The faculty consists of 4 departments, 1700 students (300 foreign students). The scientists of the faculty take part in the work of coordinating services of Ukraine.
**SYMPOSIUM PROGRAM**

Symposium program consists of three days of Plenary, Tutorial, Invited speeches; regular and short papers; and poster presentations.

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<td>Opening Speech: Five Years After</td>
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<td>Vladimir Hahanov – <em>General Chair &amp; Kharkiv National University of Radio Electronics, Ukraine</em></td>
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<tr>
<td>Addressing New Opportunities and challenges</td>
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<tr>
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<td>Program Introduction</td>
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<tr>
<td>Samvel Shoukourian – <em>Program Chair &amp; Virage Logic/Yerevan State University, Armenia</em></td>
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<td><strong>9:50–10:10</strong> Plenary Talk: “Meeting the Evolving Challenges of the Semiconductor Industry”</td>
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<td><strong>10:10–10:30</strong> Plenary talk: &quot;Challenges in the Diagnosis of Nanoelectronic Systems&quot;</td>
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<td><strong>10:30–11:00</strong> Session 2: Posters – Coffee Break</td>
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<td>Vladimir Beletskyy – <em>Tech. U. of Szczecin, Poland</em></td>
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<td>Alexander Chemeris – <em>I. of Problems of Modeling in Power Eng., Ukraine</em></td>
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<td>Jevgenyy Glushko, Vjacheslav Viter – <em>Nat. Tech. Univ. of Ukraine &quot;KPI&quot;</em></td>
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2. Graphical Method of One-Dimensional Loop Fusion in the Behavioral Description of an Application during Its Synthesis for Power Consumption Reduction  
Dmytro Lazorenko – G.E. Pukhov I. of Modeling Problems in Power Eng., NAS of Ukraine

3. A Criteria-Based Approach to Classifying Traceability Solutions  
Petro Protsyk, Konstantin Zhereb – Int. Software & Productivity Engineering Institute, Ukraine–USA

4. Automation Of Addition Of The Signature In The Database Of Destructive Objects  
Gorobets A.A. – Kharkiv Nat. U. of Radio Electronics, Ukraine

5. Processing Cores Architecture for Efficient Implementation of Digital Devices  
Olga V. Melnikova – Kharkiv Nat. U. of Radio Electronics, Ukraine

6. Synthesis of control unit with modified system of microinstructions  
Alexander Barkalov, Larysa Titarenko, Jacek Bieganowski – U. of Zielona Góra, Poland

7. Automatic Electro-Thermal Analysis in Mentor Graphics  
K.O. Petrosjanc, P.A. Kozynko – Moscow State I. of Electronics and Mathematics, Russia

Agnieszka Węgrzyn, Marek Węgrzyn – U. of Zielona Góra, Poland

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3A.1 Cadence Academic Network  
Patrick Haspel – Cadence, Germany

3B.1 How Testing Test Programs?  
Paolo Prinetto – Politecnico di Torino, Italy
**First Day: September 8th, 2007 (Saturday)**

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<th>Speaker</th>
<th>Institution</th>
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<td>Is There Still a Room For Programmers' Productivity Improvement?</td>
<td>Vladimir Pavlov</td>
<td>Intspei, Ukraine–USA</td>
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<td>Ravikumar</td>
<td>Texas Instruments, India</td>
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<td>Andre Ivanov</td>
<td>Univ of British Columbia, Canada</td>
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<td>3B.3</td>
<td>Practical Electronic Test Engineering: Education and Training in Undergraduate Setting</td>
<td>Serge Demidenko</td>
<td>Massy U., New Zealand</td>
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<td>12:00–13:00</td>
<td>Session 4A: Test Technologies</td>
<td>Moderator: Yuri Shoukourian</td>
<td>NAS RA, Armenia</td>
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<td>12:00–13:00</td>
<td>Session 4B: DFT and Fault Tolerance</td>
<td>Moderator: Bashir El-Hashimi</td>
<td>Univ of Southampton, United Kingdom</td>
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<td>12:00–13:00</td>
<td>Session 4C: Tutorial</td>
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<td>4A.1 Concurrent Error Detection Based on New Code with Modulo Weighted Transitions between Information Bits</td>
<td>Victor Mehov, Valeriy Saposnikov, Vladimir Saposnikov, Dmitriy Urganskov – Saint-Petersburg State Transport U., Russian</td>
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<td>Regular Papers</td>
<td>4B.1 Fault Tolerant and Reconfigurable System Design and Development at YCRDI: Experience and Projections for the Future</td>
<td>Arman Kuchukyan, Kima Kuchukyan – YCRDI, Armenia</td>
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<td>Writing VERILOG Test Benches using OVL Assertions</td>
<td>Zain Navabi</td>
<td>Univ of Tehran, Iran</td>
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<td>4A.2 BIST Techniques for Path Delay Fault Testing</td>
<td>4B.2 Selecting the Most Efficient DFT Techniques of Mixed-Signal Circuits Based on Economics Modeling</td>
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<td>Øystein Gjermundnes, Einar J. Aas – Norwegian U. of Science and Technology</td>
<td>Sergey G. Mosin – Vladimir State U., Russia</td>
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<th>4A.3 Analyzing Capability of LFSR Architecture as a TPG to Reduce Power, Energy and Test Delay</th>
<th>4B.3 FTARM: Fault Tolerant Asynchronous RISC Microprocessor Using Watchdog Module</th>
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<td>M. Mirzaaghatabar – Sharif U. of Technology, Iran</td>
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<td>B. Jafarpour – Amirkabir U. of Technology, Iran</td>
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<td>S. G. Miremadi – Sharif U. of Technology, Iran</td>
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<td>H. Pedram – Amirkabir U. of Technology, Iran</td>
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<td>H. Ajerlou – Sharif U. of Technology, Iran</td>
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| 4A.4     | On the Combined Use of HLDDs and EFSMs for Functional ATPG           | Giuseppe Di Guglielmo, Franco Fummi – U. of Verona, Italy  
Maksim Jenihhin – Tallinn U. of Technology, Estonia  
Graziano Pravadelli – U. of Verona, Italy  
Jaan Raik, Raimund Ubar – TUT, Estonia |
| 4B.4     | Implementing an Automatic Functional Test Pattern Generation for Mixed-Signal Boards in a Maintenance Context | Bertrand Gilles, Laurent Nana, Valérie-Anne Nicolas – Université de Bretagne Occidentale, France |
|          | Lunch                                                                 |                                                                                                             |
| 14:00–15:30 | Session 5A: Test Technology                                     | Moderator: Fabian Vargas – PUCRS, Brazil                                                                 |
|          | Session 5B: Network-on-Chip                                        | Moderator: Sybille Hellebrand – Univ of Paderborn, Germany                                                   |
|          | Regular Papers                                                      |                                                                                                             |
|          | Regular Papers                                                      |                                                                                                             |
V.A. Vardanian – Virage Logic, Armenia |
| 5B.1     | Verification of SoC Net with Core Integrity Models                  | Hayk Chukhajyan, Karen Darbinyan, Albert  
Harutyunyan, Yervant Zorian – Virage Logic, Armenia |
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<td>Andrzej Hlawiczka, Krzysztof Gucwa, Tomasz Garbolino – <em>Silesian U. of Technology, Poland</em></td>
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<td>5A.3</td>
<td>Enhancing Software Tests for COTS Systems</td>
<td>J. Sosnowski – <em>Warsaw U. of Technology, Poland</em></td>
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<td>5A.4</td>
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<td>N. Kascheev, Y. Bazhanov, P. Kascheev – <em>Nizhniy Novgorod State Technical U., Russia</em></td>
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<td>5A.5</td>
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<td>Mahshid Sedghi, Elnaz Koopahi, Armin Alaghi and Zainalabedin Navabi – <em>U. of Tehran, Iran</em></td>
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<td>5B.2</td>
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<td>Kim Petersén, Johnny Öberg – <em>Royal Inst. of Technology, Sweden</em></td>
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<td>Bengt Magnhagen – <em>School of Eng. POB, Sweden</em></td>
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<td>5B.4</td>
<td>Time-Efficient Power-Constrained Core Mapping Algorithm in NoC Based on Genetic Algorithm</td>
<td>Mohammad-Reza Binesh-Marvasti, Mohsen Saneei, Ali Afzali-Kusha, and Siamak Mohammadi – <em>U. of Tehran, Iran</em></td>
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<td>5B.5</td>
<td>High-level Analysis for Reconfiguration of a Fault Tolerant Mesh-based NoC Architecture Using Transaction Level Modeling</td>
<td>Homa Alemzadeh, Fatemeh Refan – <em>U. of Tehran, Iran</em></td>
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<td>Paolo Prinetto – <em>Politecnico di Torino, Italy</em></td>
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<td>Zainalabedin Navabi – <em>U. of Tehran, Iran</em></td>
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<tr>
<td>15:30–20:30</td>
<td>Social Program: City Tour</td>
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<td>21:00–23:00</td>
<td>Welcome Banquet: Dzoraberd Restaurant</td>
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<tr>
<td>9:30–13:00</td>
<td><strong>Social Program: Visit to Etchmidzin and surroundings</strong></td>
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<td>13:00–14:00</td>
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<tr>
<td>14:00–14:40</td>
<td><strong>Session 6: Plenary Session</strong></td>
<td>Moderator: Andre Ivanov – <em>Univ of British Columbia, Canada</em></td>
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<td></td>
<td><strong>Plenary Talk: &quot;Self Testing Embedded Systems on a Chip&quot;</strong></td>
<td>Jacob Abraham – <em>Univ of Texas at Austin, USA</em></td>
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<td>**Plenary Talk: &quot;IC Test Has and Will Remain and Exciting Area to Work&quot;</td>
<td>Rohit Kapur – <em>Synopsys, USA</em></td>
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<tr>
<td>14:40–15:40</td>
<td><strong>Session 7A: Invited Talks</strong></td>
<td>Moderator: Hans Joachim Wunderlich – <em>U. of Stuttgart, Germany</em></td>
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<tr>
<td>7A.1</td>
<td>Analog Design and Test: where are we going to?</td>
<td>Jose Luis Huertas Diaz – <em>CNM, Spain</em></td>
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<td>7A.2</td>
<td>Adaptive Power Management-aware Design for Manufacturing Test</td>
<td>Bashir El-Hashimi – <em>Univ of Southampton, UK</em></td>
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<td>7A.3</td>
<td>Reliable Nanoscale Systems - Challenges and Strategies for On- and Offline Testing</td>
<td>Sybille Hellebrand – <em>Univ of Paderborn, Germany</em></td>
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<td><strong>Session 7B: Invited Talks</strong></td>
<td>Moderator: Patrick Haspel – <em>Cadence, Germany</em></td>
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<td>7B.1</td>
<td>System On Chip (SOC) Design Pressures Reach Critical Points</td>
<td>Hazem El-Tahawy – <em>Mentor Graphics, Egypt</em></td>
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<td>7B.2</td>
<td>Physical Design using Transistor Design Automation</td>
<td>Ricardo Reis – <em>UFRGS, Brazil</em></td>
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<td>7B.3</td>
<td>&quot;Utilizing ESL Methodology: A Network Processor Case Study&quot;</td>
<td>Zain Navabi – <em>Univ of Tehran, Iran</em></td>
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<td>Session 8: Posters – Coffee Break</td>
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<tr>
<td>12. Improving the Performance of Partitioning with Judicious Initial Point Selection</td>
<td>S.A. Tahaee, A.H. Jahangir – Sharif U. of Technology, Iran</td>
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<tr>
<td>14. Synthesizable and Improved Performance System Level Design of a Sequential C++ Code Using a Rule Based Technique</td>
<td>Somayeh Malekshahi, Reyhaneh Saberi and Zainalabedin Navabi – U. of Tehran, Iran</td>
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<td>15. Developing Intrinsically Testable Asynchronous Template Models Using PSL</td>
<td>Arash Mehdizadeh, Behnam Ghavami, Hossein Pedram – Amirkabir U. of Technology, Iran</td>
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### Regular Papers

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<td><strong>9B.1</strong> Simulation and Verification Technologies</td>
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<td><strong>9A.2</strong> Optimization of Moore FSM on System-on-Chip</td>
<td><strong>9B.2</strong> KNURE and Intel Academic Program: Towards Multi-Core Enabled Design Automation Tools</td>
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<td><strong>9A.3</strong> Yield Improvement Based on Full Repair of SRAMs with Defective Redundancies</td>
<td><strong>9B.3</strong> Comparison of different high-level synthesis design flows</td>
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<td>K. Aleksanyan, V.A. Vardanian – Virage Logic, Armenia</td>
<td>Selivanov I.V. – Megratec, Russia</td>
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<td><strong>9A.4</strong> DRA: A Dynamic Reconfiguration Method for Error Recovery of RTLevel Designs</td>
<td><strong>9B.4</strong> New SystemVerilog-based functional verification methodology for high-capacity digital projects</td>
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<td>Naghmeh Karimi, and Zainalabedin Navabi – U. of Tehran, Iran</td>
<td>Rabobolyuk A.V. – Megatec, Russia</td>
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<td>9A.5</td>
<td>Design of Efficient Interconnection Network with Current-Mode Multiple-Valued Logic Circuits</td>
<td>Keivan Navi, Babak Shirpour, Nazanin Malekooty Rad – Shahid Beheshti U., Iran</td>
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<td>9A.6</td>
<td>Optimizing the Reversible Full Adder Circuit</td>
<td>Majid Mohammadi, Mohammad Eshghi, Keivan Navi – Shahid Beheshti U., Iran</td>
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| 9A.7    | Multi-version FPGA-Based NPP Instrumentation and Control Systems: Automata Models, Implementation and Operation Results | Vladimir Sklyar – State Scientific Technical Center on Nuclear and Radiation Safety, Ukraine  
Vyacheslav Kharchenko – Nat. Aerospace University “KhAI”, Ukraine  
| 9B.5    | Finding Deadlocks of Parallel Automata                             | Andrei Karatkevich – U. of Zielona Góra, Poland                                     |
| 9B.6    | On Design Of Ring LFSRs For Test Pattern Generation               | Andrzej Hlawiczka, Tomasz Garbolino – Silesian U. of Technology, Poland            |
|         | **Fault Tolerance and DFT**                                       |                                                                                     |
| 9B.7    | Memory Repair Method By Using Spares                               | Hahanov V.I., Litvinova E.I., Mostovaya K.L.  
Parfenty A.N. – Kharkiv Nat. U. of Radio Electronics, Ukraine                       |
| 9B.8    | Using SWIFI to Analyse Fault Effects in Computers                 | J. Sosnowski, P. Gawkowski – Warsaw U. of Technology, Poland                        |
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<td>9A.9</td>
<td>Implementation of the Filter 9/7 in a Software Package Matlab (Simulink)</td>
<td>Irina Hahanova, Irina Pobegenko, Maryna Kaminska, Mehdry Masud</td>
<td>Kharkiv Nat. U. of Radio Electronics, Ukraine</td>
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<tr>
<td>9A10</td>
<td>Testbench Automation for Pipelined Designs Based on Contract Specifications</td>
<td>Alexander Kamkin</td>
<td>Inst. for System Programming of Russian Academy of Sciences</td>
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<td>9A11</td>
<td>VHDL Obfuscation Techniques for Protecting Intellectual Property Rights on Design</td>
<td>M. Brzozowski, V. N. Yarmolik</td>
<td>Bialystok Technical U., Poland</td>
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<td>9A12</td>
<td>Asynchronous Behavior Related Retiming in Gated-Clock GALS Systems</td>
<td>Sam Farrokhi, Masoud Zamani, Hossein Pedram, Mehdi Sedighi</td>
<td>Amirkabir U. of Technology, Iran</td>
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<tr>
<td>9B10</td>
<td>Testable Design of Template based QDI Asynchronous Circuits</td>
<td>Masoud Zamani, Mehrdad Najibi, Hossein Pedram</td>
<td>Amirkabir U. of Technology, Iran</td>
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<td>9B11</td>
<td>An Effort-Minimized DFT Scheme for Microcontroller Aimed at In-system Test</td>
<td>Fang Bao, Yuanfu Zhao, Jun Du</td>
<td>Beijing Microelectronics Technology Inst. of China Aerospace Science and Technology Corp.</td>
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<td>9B12</td>
<td>Leakage Power Analysis of Asynchronous Pipeline Templates</td>
<td>Behnam Ghavami, Mohammad Salehi, Hossein Pedram</td>
<td>Amirkabir U. of Technology, Iran</td>
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<td>9B13</td>
<td>Low Cost SOC Synthesis</td>
<td>Mehdi Salmani-Jelodar, Faezeh Montazeri, Saeed Safari</td>
<td>U. of Tehran, Iran</td>
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<td>9B14</td>
<td>Reducing the Complexity of Partitioning Problem in High Level Synthesis</td>
<td>S.A. Tahae, A.H. Jahangir</td>
<td>Sharif U. of Technology, Iran</td>
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<td>9B15</td>
<td>Testing of Routers in NoC Mesh Architecture Using Router’s Functionality</td>
<td>Atefe Dalirsani, Zainalabedin Navabi</td>
<td>U. of Tehran, Iran</td>
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<tr>
<td>19:00–21:00</td>
<td>Social Program: Concert – Armenian Folkloric Song and Dance Ensemble</td>
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<tr>
<td>21:00–23:00</td>
<td>Dinner: Restaurant (with Full Registration)</td>
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<td>9B16</td>
<td>Fault-Tolerance through Scheduling of Periodic Tasks in Hard Real-Time Systems with Possible Software Fault</td>
<td>M. Asadi, A. Afshar, M B. Menhaj – Amirkabir U. of Technology, Iran</td>
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<td>9B17</td>
<td>Power and Performance Optimized NoC Based Systems Design Flow</td>
<td>M. Esmaeil-doust, N. Kazemi-fard, M. A. Tehrani, M. A. Taherkhani, M. Abbaspour – Shahid Beheshti U., Iran</td>
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<td>Moderator: Paolo Prinetto – Politecnico di Torino, Italy</td>
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<td></td>
<td><strong>Plenary Talk: “TRUSTED ILLIAC: A Common Hardware Framework for Reliability and Security”</strong> Ravishankar K. Iyer – University of Illinois at Urbana-Champaign, USA</td>
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<td><strong>Plenary Talk: &quot;Delivering Technologies for the Parallel Age&quot;</strong> Victor Mieres – National Instruments, Asia</td>
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<td>14:00–15:00</td>
<td><strong>Session 11A: Invited Talks</strong></td>
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<td>Moderator: Jacob Abraham – Univ of Texas at Austin, USA</td>
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<td>11A.1</td>
<td><strong>Custom Design Platforms of the Future</strong></td>
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<td>Fred Sendig – Synopsys, USA</td>
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<td>11A.2</td>
<td><strong>Trends in Management &amp; Business Processes in Semiconductor Product Development</strong></td>
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<td>Ron Collett – Numetrics, USA</td>
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<td>11A.3</td>
<td><strong>Software Agents in Diagnosis of Heterogeneous Distributed Systems</strong></td>
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<td>Liviu Miclea – Univ of Tech. Cluj, Romania</td>
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<td>14:00–15:00</td>
<td><strong>Session 11B: Invited Talks</strong></td>
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<td>Moderator: Serge Demidenko – Massy Univ., New Zealand</td>
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<td>11B.1</td>
<td><strong>Modeling Software and Hardware Defects by Dynamic Discrete Event Simulation</strong></td>
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<td>Jack Arabian – Comparative Management Associates, USA</td>
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<td>11B.2</td>
<td><strong>Embedded Signature Monitoring Based on Profiling Deployed Software Technique</strong></td>
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<td>Fabian Vargas – PUCRS, Brazil</td>
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<td>11B.3</td>
<td><strong>Combinatorial Method of Design of Quasi-Complete Fault Tolerant Networks Based on the Mathematic Block-Schema Model</strong></td>
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<td>Michael Karavay – RAS, Russia</td>
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<td>12B</td>
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<td>15:00–16:00</td>
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**Regular Papers**

9B.1 Low Power Instruction Cache Architecture Using Effective Inspector
Ming Yang, Lixin Yu – Beijing Microelectronic Technique Inst., China

**Short Papers**

12B.1 Pseudo-Ring Test RAM: Concept and Tools
G. Bodyan – Technical U. of Moldova

12B.2 On-Line Testing Method For Increasing a Reliability of the Result Checking
Drozd A., Lobachev M. – Odessa Nat. Poly. U., Ukraine
Rucinski A. – U. of New Hampshire, USA
Drozd J. – Odessa Nat. Poly. U., Ukraine

12B.3 An Efficient 2-Phase March Algorithm for Full Diagnosis of All Simple Static Faults in Random Access Memories
G. Harutunyan – Virage Logic, Armenia
H. Kocharyan – State Engineering U. of Armenia
V.A. Vardanian – Virage Logic, Armenia

**The Core Test Language (CTL): A white Board Discussion**
Rohit Kapur – Synopsys, USA
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<td>9B.2</td>
<td>A Forward-Looking Non-Search Based Synthesis Algorithm for Reversible Circuits</td>
<td>Mehdi Saeedi, Morteza Saheb Zamani, Mehdi Sedighi</td>
<td>Amirkabir U. of Technology, Iran</td>
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<td>9B.3</td>
<td>Leakage Currents and Static Power Consumption in Nanometer CMOS ICs</td>
<td>W. Kuzmicz, E. Piwowarska, A. Pfitzner and D. Kasprowicz</td>
<td>Warsaw U. of Technology, Poland</td>
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<td>Continuous Approach to Bridging Faults Modeling and Test Pattern Generation</td>
<td>N. Kascheev, F. Podyablonsky</td>
<td>Nizniy Novgorod State Technical U., Russia</td>
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<td>12B.5</td>
<td>An Evolutionary Approach to Statistical Design Space Exploration</td>
<td>Minoo Mirsaedi, Morteza Saheb Zamani</td>
<td>Amirkabir U. of Technology, Iran</td>
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<td>12B.6</td>
<td>Scalable Neural-Network Stream Processor</td>
<td>P. Saeedi, A. Naghdinezhad, H. Esmaeilzadeh, S. Mohammadi, S. M. Fakhraie</td>
<td>University of Tehran, Iran</td>
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<td>12B.7</td>
<td>Optimization of the Data Width to the Booked Quality of the Dobeshies-Wavelet Transform</td>
<td>Hahanova Irina, Barannik Vladimir, Litvinova Eugenia, Pobezhenko Irina</td>
<td>Kharkiv Nat. U. of Radio Electronics, Ukraine</td>
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<td>9B.4</td>
<td>Design of a Low Power Digital Core for a Dual Mode UHF EPC RFID Tag</td>
<td>Vahid Roostaie, Vali Najafi – KavoshCom R&amp;D Group, Iran</td>
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<td>Siamak Mohammadi – University of Tehran, Iran</td>
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<td>Ali Fotowat-Ahmady – KavoshCom R&amp;D Group, Iran</td>
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<td>12B.8</td>
<td>A Design Method of Single Event Upset Tolerant Phase Locked Loop</td>
<td>Vazgen Melikyan, Aristakes Hovsepyan, Alik Sargsyan, Grigor Harutyunyan, Rafayel Ghasabiy – Synopsys Armenia CJSC</td>
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<td>12B.9</td>
<td>Design of Reduced Quantum Cost Reversible BCD Adder</td>
<td>M. Mohamadi, M. Eshghi, A. Kaivani – Shahid Beheshti U., Iran</td>
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<td>12B.10</td>
<td>An Ultrawideband CMOS Low Noise Amplifier Design and Architectures Comparison</td>
<td>Rafayel Ghasabiy, Anahit Ghasabiy, Davit Badalyan, Artur Antonyan – Synopsys Armenia CJSC</td>
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| 12B11 Using Asynchronous Serial Transmission in Physical Design for Congestion Reduction  
Ali Jahanian, Morteza Saheb Zamani – Amirkabir U. of Technology, Iran |
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| 17. Moore FSM Synthesis with Coding of Compatible Microoperations Fields  
Alexander Barkalov, Larysa Titarenko, Alexander Barkalov, Jr. – U. of Zielona Góra, Poland |
| 18. Fault Tolerant Implementation of SpaceWire Interface in SRAM-based FPGA  
Supeng Chen and Lixin Yu – Beijing Microelectronic Technology Inst., China |
| 19. Analysis of Output Resistance Bit-wise Control Method for Memory I/Os  
William Movsisyan, Karen Sahakyan, Davit Shaghgamyan, Aristakes Hovsepyan, Davit Badalyan – Synopsys Armenia CJSC |
| 20. Improving Behavioral Synthesis In Hardware/Software Co-Design  
Mahmood Fazlali, Ali Zakerolhosseini, Mohammad K. Fallah, Sara Hashemi – Shahid Beheshti U., Iran |
| 21. A Novel Fault-Tolerant Reconfigurable NoC Architecture  
Mohammadreza Binesh Marvasti, Saeed Safari, Ali Afzali-Kusha, and Siamak Mohammadi |
| 22. Optimal Thickness of Non-diffracting Subsurface Mirrors of X-Ray Optical Memory  
Hakob (Akop) P. Bezirganyan – Yerevan State U., Armenia |
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<td><strong>Moderator:</strong> Sergey Mosin – Vladimir State University, Russia</td>
<td>Design for Yield and Reliability Yervant Zorian – Virage Logic, USA</td>
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<td>14A.3</td>
<td>Modeling and Formal Verification of Hardware Designs</td>
<td>Niusha Hakimipour, Niloofar Razavi, Marjan Sirjani – U. of Tehran, Iran</td>
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<td>Andrea Fedeli – STMicroelectronics, Italy</td>
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<td>Yiu Fai Lam – Hong Kong Inst. of Science and Technology</td>
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<td>Menouer Boubekour, Ka Lok Man, Emanuel Popovici – U. College Cork, Ireland</td>
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<td>14B.3</td>
<td>Quasioptimal Algorithm of Timing Recovery in Autocorrelation Receiver of Phase Shift Keying Signal</td>
<td>Vitaliy A. Balashov – Odessa Research Inst. of Communication, Ukraine</td>
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<td>Victor V. Panteleev – TELNET, Ltd., Ukraine</td>
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<td>Leonid M. Lyakhovetskyy – Odessa Research Inst. of Communication, Ukraine</td>
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<td>14B.4</td>
<td>A new Approach to support Fault Simulation of Delay Insensitive Asynchronous Circuits with Synchronous Toolset</td>
<td>M. Mirzaaghatabar – Sharif U. of Technology, Iran</td>
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<td>A. Rasooli, B. Ghavami – Amirkabir U. of Technology, Iran</td>
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<td>Sh. Hessabi – Sharif U. of Technology, Iran</td>
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### Short Papers

**14A.5 A Roadmap Towards Microelectronics Education in the Global Era**
Andrzej Rucinski, Don Bouldin – *U. of New Hampshire, USA*
Thaddeus Kochanski – *U. of Tennessee, USA*

**14A.6 Graphical System Design Technology Accelerating the Modern Development Cycle**
David Wilson, Aram Salatian – *National Instruments*

**14A.7 Toward Embedded Emotionally Intelligent System**

**14B.5 Genetic Algorithms for Fault Dictionary Size Reduction**
D. Speranskiy, S. Mironov – *Saratov State U., Russia*

**14B.6 An Algorithm for Analysis of Analog Parts of Circuits Described in VHDL-AMS**
Arezoo Kamran, Amir Hossein Jahangir – *Sharif U. of Technology, Iran*

**14B.7 A Compact SOI/SOS MOSFET Macromodel Accounting for Radiation Effects**
K. O. Petrosjanc, I. A. Kharitonov, E. V. Orekhov, L. M. Sambursky – *Moscow U. of Electronics and Mathematics, Russia*
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<th>Session</th>
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<th>Authors</th>
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<td>14A.8</td>
<td>PeNCAD System – From Modeling to Synthesis of Concurrent Controllers</td>
<td>Agnieszka Węgrzn, Marek Węgrzn – U. of Zielona Góra, Poland</td>
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<td>14A.9</td>
<td>A Software Tool for Generation of March Algorithms for Faults in SRAMs</td>
<td>G. Harutunyan – Virage Logic, Armenia</td>
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<td>14B.8</td>
<td>A Heuristic Method for Instruction-Set Extension Generation</td>
<td>Payman Loloeyan, Maghsoud Abbaspour – Shahid Beheshti U., Iran</td>
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<td>14B10</td>
<td>Detect Interfacial Cracks Based on Thermal Contact Resistance for Composite Materials</td>
<td>Chun-Yin Wu, Wen-Chang Lin – Tatung U., Taiwan</td>
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### Third Day: September 10th, 2007 (Monday)

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<th>14A11 Processor Description in APDL for Design Space Exploration of Embedded Processors</th>
<th>14B11 Diagnosis Method of Malicious Code in Executable Files</th>
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<td>N. Honarmand, H. Sohofi – U. of Tehran, Iran</td>
<td>Saprykin Aleksandr, Kiktenko Vitaly, Galagan Sergey, Kunitsky Artem – Kharkiv Nat. U. of Radio Electronics, Ukraine</td>
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<td>M. Abbaspour – Shahid Beheshti U., Iran</td>
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<td>Z. Navabi – U. of Tehran, Iran</td>
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<tr>
<th>18:30–19:00</th>
<th>Session 15: Closing Session</th>
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<td>Yervant Zorian, Vladimir Hahanov</td>
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| 20:00–22:00 | Dinner: Restaurant (with Full Registration) |

### Fourth Day: September 11th, 2007 (Tuesday)

Social Program: Optional Day Trip to Lake Sevan
SOCIAL PROGRAM

We hope that, regardless of the very tight time schedule, the symposium will create the opportunity not only for the exchange of scientific ideas but for some sightseeing as well.

**September 7. Optional Tour to Khor Virap and Noravank.**

The optional day tour includes a bus tour to the southern Armenia visiting beautiful monastery Khor Virap with close proximity and spectacular view to Mount Ararat. The tour continues to cross the larger agricultural area to the south well known with its grape yards, where a guided wine tour in Areni village will be organized (tasting wine, grapes and cheese), continued with a visit to Gladzor University Museum (a University from 13th century), Noravank Monastery (http://en.wikipedia.org/wiki/Noravank, a 13th century Armenian Apostolic Church Monastery) and a late lunch in a cave at Noravank canyon.

**September 8. City Tour (Manuscript Museum, Cognac Factory, Tsitsernakaberd, Hayordats Toun).**

City Tour including visit to Matenadaran (Manuscript museum), Tsitsernakaberd (Genocide museum), and Hayordats Toun – This tour will include a bus tour around the city exposing its beauty and welcoming the participants at one of the oldest cities in the world, 2700 years of age. The nowadays Yerevan however has all of the attributes of any modern European city with lots of very nice cafes, restaurants, fashionable shops and parks.

The city has a circular shape having the “Opera House Circle” in the very center from which different rays of streets and avenues head to different corners of the city. At the edges the city slowly turns in to squares forming the rural areas. The center is quite beautiful especially in the time of year the conference is being held at, with a lot of colors in the streets. The architecture of the center of the city is mostly 5 story-buildings made from beautiful red brick-stone. In the new constructed avenue, however one might find tall building made from concrete.

The visit would include, the Manuscript museum, where one can see lots of old writing and original Bible writing. The Genocide museum, Tsitsernakaberd, has also a special place in the tour which will take us away from the center up to one of the hills of the city on a
big plateau with beautiful sight of the city. During the tour we will also see the houses of Parliament, the Presidential white house and much more.

**September 9. Visit to Etchmiadzin and surroundings.**

Etchmiadzin – is the holiest city in Armenia and the headquarters of the katholikos, the head of the Armenian Apostolic Church. It is in the Armavir province, about 20 km west of Yerevan. The main place of interest there is of course the holy church of Etchmiadzin built in 301 AD, when Saint Grigor Lusavorich (Saint Gregory the Illuminator) pointed to the exact place on the land where it should be built.

**September 10. Tour to Garni/Geghart (pegan temple and rock carved monastery).**

Garni – Geghard – The pagan temple of Garni is a very nice temple in the region of which one can find facts of the so-long history of the Armenian Nation such as fortifications of the 3-rd millennium BC.

The church of Geghard is a unique architectural construction in the Kotayk province of Armenia, being partially carved out of the adjacent mountain, surrounded by cliffs. It is listed as a UNESCO World Heritage Site.

**September 11. Optional Tour to Lake Sevan and Haghartsin.**

The optional day tour including a visit to the largest lake in Armenia called Sevan, which is one of the largest high-altitude lakes in the world.

The tour continues to the north-eastern region of Armenia visiting beautiful monastery Haghartsin, that was built between 10th and 14th centuries under patronage of Bagratouni Dynasty of Armenian Kingdom.

The conference will offer a very rich and full social program at a full registration fee, however if You prefer to explore the city and/or country on your own please contact Tigran Atoyan at tigran.atoyan@viragelogic.com or directly during the conference and a tour of your choice will be organized.