



FROM THE ORGANIZING COMMITTEE

We have a great pleasure to invite you to IEEE EAST-WEST DESIGN & TEST SYMPOSIUM – EWDTs'07!

The purpose of the symposium is to coordinate and exchange experiences between leading scientific schools and experts of the Eastern and Western Europe as well as of the USA in the field of digital systems design and testing.

From the one side, an overview of the state-of-the-art and of the most important progress trends of the industrial design and test will be presented by western researchers.

On the other side, an overview of achievements and research results obtained by the scientists of the post socialistic states during the last five years will be presented by the researchers from Eastern countries.

We are happy that EWDTs is becoming a world known as we have seen the interest of Eastern and Western European scientists in mutual collaboration. As a result of this collaboration we can see the penetration of new technologies to the market of Eastern Europe and to the university education. The feedback is determined by inputs of West-European scientists in research activities of Europe and USA.

We would like to thank: Yervant Zorian, Raimund Ubar, Andre Ivanov, Samvel Shoukourian (with the Armenian team), Zainalabedin Navabi (with the large Tehran team), Lyudmila Nesterenko, Vladimir Pavlov and Alexander Ryjov for taking an active part in organization of the conference, for financial, technical support, for international activity in Ukraine in the field of higher education, overall support of the university, support in preparation and holding of the symposium. The greatest appreciation to all official EWDTs'07 sponsors (Cadence, Echostar, Intel, INTSPEI, Mentor Graphics, National Instruments, Synopsys, Virage Logic) provided the best quality of financial support. We especially thank the Rector of Kharkov National University of Radio Electronics, Professor Mikhail Bondarenko, for overall support and active personal participation in preparation and holding of the symposium. Also we thank all contributors for high-level technical program and presentations.

Finally, we welcome all the participants of the EWDT'07 symposium and wish you successful discussions and a pleasant stay in Yerevan!

EWDTs'07 Organizing Committee



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IEEE DESIGN & TEST OF COMPUTERS



IEEE D&T is a bimonthly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers, and researchers. D&T features peer-reviewed original work describing methods and



practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

- System Level Design and Test
- Embedded Test Technology
- Low Power Design
- Reconfigurable Systems
- Board and System Test
- Analog and Mixed Signal Design and Test
- System-on-Chip Design and IP Reuse
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- May/June: IR-Drop and Power Supply Noise Effects on Design and Test
- July/August: Special Section on CAD for Emerging Technologies
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Tallinn University of Technology
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GENERAL INFORMATION AND INQUIRIES

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BANKING

Generally, everywhere in Armenia you pay in Armenian drams (AMD). The currency units are: dram and luma. 1 AMD = 100 luma. The Armenian dram is a fully convertible currency internally in Armenia.

Foreign currency exchange facilities are available at major airports, railway stations, at large hotels, as well as in many private offices, called "Currency exchange". Credit cards can be used in such places as banks and branch banks. Approximate currency exchange rate: 1 USD = 337 AMD, 1 EURO = 458 AMD.

CREDIT CARDS: Visa Card and Master Card are the most common cards. However, other cards are also accepted.

PROGRAM OF THE SYMPOSIUM

The program of the EWDTTS'07 symposium will consist of oral presentations of contributed and invited papers, tutorial lectures, regular and short papers. The language of the conference is English, neither translation nor interpretation will be provided.

The time for oral presentations of regular papers is 15 minutes for presentation and discussion; short paper is 5 minutes.

WEATHER

September in Yerevan is generally sunny. The temperature can be typically 28 deg C during days. During nights, the temperature can drop to 18-22 deg C.



GENERAL INFORMATION

Total number of authors: 353.

Number of papers: 152.

Preliminary number of participants: 150.

Number of countries: 32 (*Algeria, Armenia, Australia, Bangladesh, Brazil, Canada, Egypt, Estonia, France, Germany, Hong-Kong, India, Iran, Ireland, Italy, Jordan, Moldova, Nigeria, Norway, Pakistan, Poland, Romania, Russia, Saudi Arabia, Spain, Syria, Sweden, Taiwan, UK, Ukraine, USA*).

KHARKIV NATIONAL UNIVERSITY OF RADIO ELECTRONICS



Kharkov National University of Radio Electronics (www.kture.kharkov.ua) was founded 77 years ago. It was the best University in USSR in 70th – 90th in the field of radio electronics. Today the University is the leader among all technical universities of Ukraine. Total number of students is more than 11000. The number of PhD and Doctoral students is more than 250. There are 650



teachers working for University. Among them there are 150 professors and 450 PhD. The laboratories of the University are equipped with more than 1100 computers.

Every year the University graduates more than 1832 bachelors, 1537 specialists, 184 masters. Graduate students of the University work in USA, Germany, England, Finland, France, Poland, Russia, Bulgaria.

The University has close contacts with universities from the following countries: Germany, USA, UK, France, Japan, China, Bulgaria, Finland, the Netherlands, Greece, Russia, Byelorussia, Czech Republic, Mexico, Serbia.

There are 50 contracts with the universities of other countries.

The University has obtained 67 grants during 2006/2007 years.

Scientific activity:

In 2006/2007 academic years 54 PhD theses and 12 doctoral theses were defended.

During 2004/2005 there were made more than 1000 publications. Among them are:

- 290 scientific articles;
- 550 thesis;
- 15 textbooks;
- 160 manuals.

The University publishes 5 periodicals. In 2006/2007 5 international conferences and workshops were organized by the University.

The University consists of 7 faculties. The faculty of Computer Engineering and Control is one of the best not only in the university but among other technical universities, which have similar specialties. During last ten years it has been taking an active part in scientific activities of state in the field of computer systems and nets design and application. The faculty consists of 4 departments, 1700 students (300 foreign students). The scientists of the faculty take part in the work of coordinating services of Ukraine.

SYMPOSIUM PROGRAM

Symposium program consists of three days of Plenary, Tutorial, Invited speeches; regular and short papers; and poster presentations.

First Day: September 8th, 2007 (Saturday)	
9:00–10:30	Session 1: Opening Session Moderator: Vladimir Hahanov
	Opening Speech: Five Years After Vladimir Hahanov – <i>General Chair & Kharkiv National University of Radio Electronics, Ukraine</i> Addressing New Opportunities and challenges Yervant Zorian – <i>General chair & Virage Logic, USA</i> Program Introduction Samvel Shoukourian – <i>Program Chair & Virage Logic/Yerevan State University, Armenia</i> Short Welcome Messages
9:50–10:10	Plenary Talk: “Meeting the Evolving Challenges of the Semiconductor Industry” Magdy Abadir – <i>Freescale, USA</i>
10:10–10:30	Plenary talk: "Challenges in the Diagnosis of Nanoelectronic Systems" Hans Joachim Wunderlich – <i>Univ of Stuttgart, Germany</i>
10:30–11:00	Session 2: Posters – Coffee Break
	1. A VHDL Model of RISC Processor For Embedded Systems Vladimir Beletsky – <i>Tech. U. of Szczecin, Poland</i> Alexander Chemeris – <i>I. of Problems of Modeling in Power Eng., Ukraine</i> Jevgenyy Glushko, Vjacheslav Viter – <i>Nat. Tech. Univ. of Ukraine "KPI"</i>

First Day: September 8th, 2007 (Saturday)

2. Graphical Method of One-Dimensional Loop Fusion in the Behavioral Description of an Application during Its Synthesis for Power Consumption Reduction

Dmytro Lazorenko – *G.E. Pukhov I. of Modeling Problems in Power Eng., NAS of Ukraine*

3. A Criteria-Based Approach to Classifying Traceability Solutions

Petro Protsyk, Konstantin Zhereb – *Int. Software & Productivity Engineering Institute, Ukraine–USA*

4. Automation Of Addition Of The Signature In The Database Of Destructive Objects

Gorobets A.A. – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

5. Processing Cores Architecture for Efficient Implementation of Digital Devices

Olga V. Melnikova – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

6. Synthesis of control unit with modified system of microinstructions

Alexander Barkalov, Larysa Titarenko, Jacek Bieganowski – *U. of Zielona Góra, Poland*

7. Automatic Electro-Thermal Analysis in Mentor Graphics

K.O. Petrosjanc, P.A. Kozynko – *Moscow State I. of Electronics and Mathematics, Russia*

8. On Textual Specification of Petri Nets for Control Algorithms

Agnieszka Węgrzyn, Marek Węgrzyn – *U. of Zielona Góra, Poland*

11:00–12:00 Session 3A: Invited Talks

Moderator: Arman Kuchukian – *YCRDI, Armenia*

3A.1 Cadence Academic Network

Patrick Haspel – *Cadence, Germany*

11:00–12:00 Session 3B: Invited Talks

Moderator: Jose Luis Huertas Diaz – *CNM, Spain*

3B.1 How Testing Test Programs?

Paolo Prinetto – *Politecnico di Torino, Italy*

First Day: September 8th, 2007 (Saturday)

<p>3A.2 Is There Still a Room For Programmers' Productivity Improvement? Vladimir Pavlov – <i>Intspei, Ukraine–USA</i></p> <p>3A.3 Power Infrastructure Aware Test Generation for System-on-Chip Ravikumar – <i>Texas Instruments, India</i></p>	<p>3B.2 50 Years To Go From The First ICs To Systems Of Systems On Chip – How Did And Will Test Technology Keep Up? Andre Ivanov – <i>Univ of British Columbia, Canada</i></p> <p>3B.3 Practical Electronic Test Engineering: Education and Training in Undergraduate Setting Serge Demidenko – <i>Massy U., New Zealand</i></p>	
<p>12:00–13:00 Session 4A: Test Technologies Moderator: Yuri Shoukourian – <i>NAS RA, Armenia</i></p>	<p>12:00–13:00 Session 4B: DFT and Fault Tolerance Moderator: Bashir El-Hashimi – <i>Univ of Southampton, United Kingdom</i></p>	<p>12:00–13:00 Session 4C: Tutorial</p>
<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>4A.1 Concurrent Error Detection Based on New Code with Modulo Weighted Transitions between Information Bits Victor Mehov, Valeriy Saposhnikov, Vladimir Saposhnikov, Dmitriy Urganskov – <i>Saint-Petersburg State Transport U., Russian</i></p>	<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>4B.1 Fault Tolerant and Reconfigurable System Design and Development at YCRDI: Experience and Projections for the Future Arman Kuchukyan, Kima Kuchukyan – <i>YCRDI, Armenia</i></p>	<p>Writing VERILOG Test Benches using OVL Assertions Zain Navabi – <i>Univ of Tehran, Iran</i></p>

First Day: September 8th, 2007 (Saturday)

4A.2BIST Techniques for Path Delay Fault Testing

Øystein Gjermundnes, Einar J. Aas – *Norwegian U. of Science and Technology*

4A.3Analyzing Capability of LFSR Architecture as a TPG to Reduce Power, Energy and Test Delay

Mehdi Kamal, Somayyeh Koohi, Shaahin Hessabi – *Sharif U. of Technology, Iran*

4B.2 Selecting the Most Efficient DFT Techniques of Mixed-Signal Circuits Based on Economics Modeling

Sergey G. Mosin – *Vladimir State U., Russia*

4B.3 FTARM: Fault Tolerant Asynchronous RISC Microprocessor Using Watchdog Module

M. Mirzaaghatabar – *Sharif U. of Technology, Iran*

B. Jafarpour – *Amirkabir U. of Technology, Iran*

S. G. Miremadi – *Sharif U. of Technology, Iran*

H. Pedram – *Amirkabir U. of Technology, Iran*

H. Ajerlou – *Sharif U. of Technology, Iran*

First Day: September 8th, 2007 (Saturday)

<p>4A.4 On the Combined Use of HLDDs and EFSMs for Functional ATPG Giuseppe Di Guglielmo, Franco Fummi – <i>U. of Verona, Italy</i> Maksim Jenihhin – <i>Tallinn U. of Technology, Estonia</i> Graziano Pravadelli – <i>U. of Verona, Italy</i> Jaan Raik, Raimund Ubar – <i>TUT, Estonia</i></p>	<p>4B.4 Implementing an Automatic Functional Test Pattern Generation for Mixed-Signal Boards in a Maintenance Context Bertrand Gilles, Laurent Nana, Valérie-Anne Nicolas – <i>Université de Bretagne Occidentale, France</i></p>	
<p>13:00–14:00 Lunch</p>		
<p>14:00–15:30 Session 5A: Test Technology Moderator: Fabian Vargas – <i>PUCRS, Brazil</i></p>	<p>14:00–15:30 Session 5B: Network-on-Chip Moderator: Sybille Hellebrand – <i>Univ of Paderborn, Germany</i></p>	
<p>Regular Papers</p> <hr/> <p>5A.1 Fast Generation of March Tests for Fault Detection and Diagnosis in Static Random Access Memories T.A. Gyonjyan, J.T. Sargsyan – <i>Yerevan State U., Armenia</i> V.A. Vardanian – <i>Virage Logic, Armenia</i></p>	<p>Regular Papers</p> <hr/> <p>5B.1 Verification of SoC Net with Core Integrity Models Hayk Chukhajyan, Karen Darbinyan, Albert Harutyunyan, Yervant Zorian – <i>Virage Logic, Armenia</i></p>	

First Day: September 8th, 2007 (Saturday)

5A.2 On Application of Ring LFSRs for Interconnect Testing

Andrzej Hlawiczka, Krzysztof Gucwa, Tomasz Garbolino – *Silesian U. of Technology, Poland*

5A.3 Enhancing Software Tests for COTS Systems

J. Sosnowski – *Warsaw U. of Technology, Poland*

5A.4 Efficient Use of the Continuous Approach for Test Generation of Benchmark Circuits

N. Kascheev, Y. Bazhanov, P. Kascheev – *Nizhniy Novgorod State Technical U., Russia*

5A.5 An Exhaustive Test Strategy Based on Flooding Routing for NoC Switch Testing

Mahshid Sedghi, Elnaz Koopahi, Armin Alaghi and Zainalabedin Navabi – *U. of Tehran, Iran*

5B.2 Towards an Almost C-Testable NoC Test Strategy

Kim Petersén, Johnny Öberg – *Royal Inst. of Technology, Sweden*

Bengt Magnhagen – *School of Eng. POB, Sweden*

5B.3 A Heuristic Search Algorithm for Re-routing of On-Chip Networks in The Presence of Faulty Links and Switches

Nima Honarmand, Ali Shahabi and Zain Navabi – *U. of Tehran, Iran*

5B.4 Time-Efficient Power-Constrained Core Mapping Algorithm in NoC Based on Genetic Algorithm

Mohammad-Reza Binesh-Marvasti, Mohsen

Saneei, Ali Afzali-Kusha, and Siamak Mohammadi

– *U. of Tehran, Iran*

5B.5 High-level Analysis for Reconfiguration of a Fault Tolerant Mesh-based NoC Architecture Using Transaction Level Modeling

Homa Alemzadeh, Fatemeh Refan – *U. of Tehran, Iran*

Paolo Prinetto – *Politecnico di Torino, Italy*

Zainalabedin Navabi – *U. of Tehran, Iran*

First Day: September 8th, 2007 (Saturday)

**5A.6 Multi run Transparent March PNPSFk
Memory Test**
V.N. Yarmolik, I Mrozek, E. Buslowska – *Bialystok
Technical U., Poland*

Short Paper (out of schedule)

**5A.8 An Experiment on Quantitative Estimation
of Semantic Similarity between Software
Requirements**
Anatoliy Doroshenko – *Intspei, Ukraine-USA*
Olena Yatsenko – *Inst. of Software Systems of
NAS of Ukraine*

**5B.6 A Mechanism for Providing Congestion
Free Traffic Flow in Networks on Chip**
Vazgen Melikyan, Aram Martirosyan, Arshavir
Matevosyan, Samvel Chobanyan – *Synopsys
Armenia CJSC*

15:30–20:30 **Social Program: City Tour**

21:00–23:00 **Welcome Banquet: Dzoraberd Restaurant**

Second Day: September 9th, 2007 (Sunday)

9:30–13:00	Social Program: Visit to Etchmidzin and surroundings	
13:00–14:00	Lunch	
14:00–14:40	Session 6: Plenary Session Moderator: Andre Ivanov – <i>Univ of British Columbia, Canada</i>	
	Plenary Talk: "Self Testing Embedded Systems on a Chip" Jacob Abraham – <i>Univ of Texas at Austin, USA</i>	
	Plenary Talk: "IC Test Has and Will Remain and Exciting Area to Work" Rohit Kapur – <i>Synopsys, USA</i>	
14:40–15:40	Session 7A: Invited Talks Moderator: Hans Joachim Wunderlich – <i>U. of Stuttgart, Germany</i>	Session 7B: Invited Talks Moderator: <i>Patrick Haspel – Cadence, Germany</i>
7A.1	Analog Design and Test: where are we going to? Jose Luis Huertas Diaz – <i>CNM, Spain</i>	7B.1 System On Chip (SOC) Design Pressures Reach Critical Points Hazem El-Tahawy – <i>Mentor Graphics, Egypt</i>
7A.2	Adaptive Power Management-aware Design for Manufacturing Test Bashir El-Hashimi – <i>Univ of Southampton, UK</i>	7B.2 Physical Design using Transistor Design Automation Ricardo Reis – <i>UFRGS, Brazil</i>
7A.3	Reliable Nanoscale Systems - Challenges and Strategies for On- and Offline Testing Sybille Hellebrand – <i>Univ of Paderborn, Germany</i>	7B.3 "Utilizing ESL Methodology: A Network Processor Case Study" Zain Navabi – <i>Univ of Tehran, Iran</i>

Second Day: September 9th, 2007 (Sunday)

15:40–16:10 **Session 8: Posters – Coffee Break**

9. Components Visualization Approach for FPGA-based Projects Verification

Kulanov Vitaliy, Kharchenko Vyacheslav – *Nat. Aerospace U. "KhAI", Ukraine*

10. Retransmission Meter Processes Simulation System

Vdovychenko Y.I. – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

11. Using of Production Systems and Binary Relations in Expert Systems for Diagnosis of Computer Equipment

Habes A.A. Zidat – *Kharkov Nat. U. of Radio Electronics, Ukraine*

12. Improving the Performance of Partitioning with Judicious Initial Point Selection

S.A. Tahae, A.H. Jahangir – *Sharif U. of Technology, Iran*

13. Performance Evaluation on a Modified Multi Ring Algorithm for Mutual Exclusion in Distributed Systems

M. Esmaeildoust, N. Kazemifard, M. Abbaspour, A. T. Haghighat – *Shahid Beheshti U., Iran*

14. Synthesizable and Improved Performance System Level Design of a Sequential C++ Code Using a Rule Based Technique

Somayeh Malekshahi, Reyhaneh Saberi and Zainalabedin Navabi – *U. of Tehran, Iran*

15. Developing Intrinsically Testable Asynchronous Template Models Using PSL

Arash Mehdizadeh, Behnam Ghavami, Hossein Pedram – *Amirkabir U. of Technology, Iran*

Second Day: September 9th, 2007 (Sunday)

<p>16:10–18:30 Session 9A: Design Moderator: Liviu Miclea – <i>Univ of Tech. Cluj, Romania</i></p>	<p>16:10–18:30 Session 9B: Misc Topics Moderator: Alexander Drozd – <i>Odessa Nat. Polytechnic U., Ukraine</i></p>
<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>9A.1 The Design of Pulse Width Distortion Controller for High-Speed I/O Applications William Movsisyan, Vazgen Meliqyan, Davit Shaghgamyán, Davit Petrosyan, Karen Sahakyan – <i>Synopsys, Armenia</i></p> <p>9A.2 Optimization of Moore FSM on System-on-Chip Alexander Barkalov, Larysa Titarenko, Sławomir Chmielewski – <i>U. of Zielona Góra, Poland</i></p> <p>9A.3 Yield Improvement Based on Full Repair of SRAMs with Defective Redundancies K. Aleksanyan, V.A. Vardanian – <i>Virage Logic, Armenia</i></p> <p>9A.4 DRA: A Dynamic Reconfiguration Method for Error Recovery of RTL Level Designs Naghmeh Karimi, and Zainalabedin Navabi – <i>U. of Tehran, Iran</i></p>	<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>9B.1 Simulation and Verification Technologies Vladimir Hahanov, Anna Hahanova, Volodymyr Obrizan, Wajeb Gharibi – <i>Kharkiv Nat. U. of Radio Electronics, Ukraine</i></p> <p>9B.2 KNURE and Intel Academic Program: Towards Multi-Core Enabled Design Automation Tools Volodymyr Obrizan, Vladimir Hahanov – <i>Kharkiv Nat. U. of Radio Electronics, Ukraine</i></p> <p>9B.3 Comparison of different high-level synthesis design flows Selivanov I.V. – <i>Megratec, Russia</i></p> <p>9B.4 New SystemVerilog-based functional verification methodology for high-capacity digital projects Rabobolyuk A.V. – <i>Megratec, Russia</i></p>

Second Day: September 9th, 2007 (Sunday)

<p>9A.5 Design of Efficient Interconnection Network with Current-Mode Multiple-Valued Logic Circuits Keivan Navi, Babak Shirpour, Nazanin Malekooty Rad – <i>Shahid Beheshti U., Iran</i></p> <p>9A.6 Optimizing the Reversible Full Adder Circuit Majid Mohammadi, Mohammad Eshghi, Keivan Navi – <i>Shahid Beheshti U., Iran</i></p> <p>9A.7 Multi-version FPGA-Based NPP Instrumentation and Control Systems: Automata Models, Implementation and Operation Results Vladimir Sklyar – <i>State Scientific Technical Center on Nuclear and Radiation Safety, Ukraine</i> Vyacheslav Kharchenko – <i>Nat. Aerospace University “KhAI”, Ukraine</i> Eugene Bahmach, Alexander Siora, Victor Tokarev, Victor Golovir, Alexander Herasimenko – <i>Corp. “Rady”, Ukraine</i></p>	<p>9B.5 Finding Deadlocks of Parallel Automata Andrei Karatkevich – <i>U. of Zielona Góra, Poland</i></p> <p>9B.6 On Design Of Ring LFSRs For Test Pattern Generation Andrzej Hlawiczka, Tomasz Garbolino – <i>Silesian U. of Technology, Poland</i></p> <p>Fault Tolerance and DFT</p> <hr/> <p>Short Papers</p> <hr style="border-top: 1px dashed black;"/> <p>9B.7 Memory Repair Method By Using Spares Hahanov V.I., Litvinova E.I., Mostovaya K.L. Parfenty A.N. – <i>Kharkiv Nat. U. of Radio Electronics, Ukraine</i></p> <p>9B.8 Using SWIFI to Analyse Fault Effects in Computers J. Sosnowski, P. Gawkowski – <i>Warsaw U. of Technology, Poland</i></p> <p>9B.9 An Improved Implementation of the Simulated Annealing Based Standard Cell Placement Algorithm Dragon Kirill Korniyakov, Nina Kurina, Iosif Meyerov, Artem Zhivoderov – <i>N.I. Lobachevsky State U. of Nizhni Novgorod, Russia</i></p>
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Second Day: September 9th, 2007 (Sunday)

Short Papers

9A.8 Image Encoding Design Based On 2-D Combinatory Transformation

V. Hahanov, V. Barannik, A. Krasovskaya, M. Rudakova, Wade Ghribi – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

9A.9 Implementation of the Filter 9/7 in a Software Package Matlab (Simulink)

Irina Hahanova, Irina Pobegenko, Maryna Kaminska, Mehedy Masud – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

9A10 Testbench Automation for Pipelined Designs Based on Contract Specifications

Alexander Kamkin – *Inst. for System Programming of Russian Academy of Sciences*

9A11 VHDL Obfuscation Techniques for Protecting Intellectual Property Rights on Design

M. Brzozowski, V. N. Yarmolik – *Bialystok Technical U., Poland*

9A12 Asynchronous Behavior Related Retiming in Gated-Clock GALS Systems

Sam Farrokhi, Masoud Zamani, Hossein Pedram, Mehdi Sedighi – *Amirkabir U. of Technology, Iran*

9B10 Testable Design of Template based QDI Asynchronous Circuits

Masoud Zamani, Mehrdad Najibi, Hossein Pedram – *Amirkabir U. of Technology, Iran*

9B11 An Effort-Minimized DFT Scheme for Microcontroller Aimed at In-system Test

Fang Bao, Yuanfu Zhao, Jun Du – *Beijing Microelectronics Technology Inst. of China Aerospace Science and Technology Corp.*

9B12 Leakage Power Analysis of Asynchronous Pipeline Templates

Behnam Ghavami, Mohammad Salehi, Hossein Pedram – *Amirkabir U. of Technology, Iran*

9B13 Low Cost SOC Synthesis

Mehdi Salmani-Jelodar, Faezeh Montazeri, Saeed Safari – *U. of Tehran, Iran*

9B14 Reducing the Complexity of Partitioning Problem in High Level Synthesis

S.A. Tahaei, A.H. Jahangir – *Sharif U. of Technology, Iran*

9B15 Testing of Routers in NoC Mesh Architecture Using Router's Functionality

Atefe Dalirsani, Zainalabedin Navabi – *U. of Tehran, Iran*

Second Day: September 9th, 2007 (Sunday)

**9A13 Web-Based Computer Aided Design
Support of Finite State Machine Additive
Decomposition for Low Power**
Alexander Sudnitson, Sergei Devadze – TUT, Estonia

**9B16 Fault-Tolerance through Scheduling of
Periodic Tasks in Hard Real-Time Systems
with Possible Software Fault**
*M. Asadi, A. Afshar, M B. Menhaj – Amirkabir U. of
Technology, Iran*

**9B17 Power and Performance Optimized NoC
Based Systems Design Flow**
*M. Esmail-doust, N. Kazemi-fard, M. A. Tehrani,
M. A. Taherkhani, M. Abbaspour – Shahid
Beheshti U., Iran*

19:00–21:00 **Social Program: Concert – Armenian Folkloric Song and Dance Ensemble**

21:00–23:00 **Dinner: Restaurant** (with Full Registration)

Third Day: September 10th, 2007 (Monday)

8:30–12:00 **Social Program: Tour to Garni/Geghart**

12:20–13:00 **Session 10: Plenary Session**
 Moderator: Paolo Prinetto – *Politecnico di Torino, Italy*

Plenary Talk: “TRUSTED ILLIAC: A Common Hardware Framework for Reliability and Security”
 Ravishankar K. Iyer – *University of Illinois at Urbana-Champaign, USA*

Plenary Talk: "Delivering Technologies for the Parallel Age"
 Victor Mieres – *National Instruments, Asia*

13:00–14:00 **Lunch**

14:00–15:00 **Session 11A: Invited Talks**
 Moderator: Jacob Abraham – *Univ of Texas at Austin, USA*

14:00–15:00 **Session 11B: Invited Talks**
 Moderator: Serge Demidenko – *Massy Univ., New Zealand*

11A.1 Custom Design Platforms of the Future
 Fred Sendig – *Synopsys, USA*

11B.1 Modeling Software and Hardware Defects by Dynamic Discrete Event Simulation
 Jack Arabian – *Comparative Management Associates, USA*

11A.2 Trends in Management & Business Processes in Semiconductor Product Development
 Ron Collett – *Numetrics, USA*

11B.2 Embedded Signature Monitoring Based on Profiling Deployed Software Technique
 Fabian Vargas – *PUCRS, Brazil*

11A.3 Software Agents in Diagnosis of Heterogeneous Distributed Systems
 Liviu Miclea – *Univ of Tech. Cluj, Romania*

11B.3 Combinatorial Method of Design of Quasi-Complete Fault Tolerant Networks Based on the Mathematic Block-Schema Model
 Michael Karavay – *RAS, Russia*

Third Day: September 10th, 2007 (Monday)

<p>15:00–16:00 Session 12A: Low Power Moderator: Hazem El-Tahawy – <i>Mentor Graphics, Egypt</i></p>	<p>15:00–16:00 Session 12B: Test Technology Moderator: Michael Karavay – <i>RAS, Russia</i></p>	<p>15:00–16:00 Session 12C: Tutorial</p>
<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>9B.1 Low Power Instruction Cache Architecture Using Effective Inspector Ming Yang, Lixin Yu – <i>Beijing Microelectronic Technique Inst., China</i></p>	<p>Short Papers</p> <hr style="border-top: 1px dashed black;"/> <p>12B.1 Pseudo-Ring Test RAM: Concept and Tools G. Bodyan – <i>Technical U. of Moldova</i></p> <p>12B.2 On-Line Testing Method For Increasing a Reliability of the Result Checking Drozd A., Lobachev M. – <i>Odessa Nat. Poly. U., Ukraine</i> Rucinski A. – <i>U. of New Hampshire, USA</i> Drozd J. – <i>Odessa Nat. Poly. U., Ukraine</i></p> <p>12B.3 An Efficient 2-Phase March Algorithm for Full Diagnosis of All Simple Static Faults in Random Access Memories G. Harutunyan – <i>Virage Logic, Armenia</i> H. Kocharyan – <i>State Engineering U. of Armenia</i> V.A. Vardanian – <i>Virage Logic, Armenia</i></p>	<p>The Core Test Language (CTL): A white Board Discussion Rohit Kapur – <i>Synopsys, USA</i></p>

Third Day: September 10th, 2007 (Monday)

9B.2 A Forward-Looking Non-Search Based Synthesis Algorithm for Reversible Circuits

Mehdi Saeedi, Morteza Saheb Zamani, Mehdi Sedighi – *Amirkabir U. of Technology, Iran*

9B.3 Leakage Currents and Static Power Consumption in Nanometer CMOS ICs

W. Kuzmicz, E. Piwowarska, A. Pfitzner and D. Kasprowicz – *Warsaw U. of Technology, Poland*

12B.4 Continuous Approach to Bridging Faults Modeling and Test Pattern Generation

N. Kascheev, F. Podyablonsky – *Nizniy Novgorod State Technical U., Russia*

12B.5 An Evolutionary Approach to Statistical Design Space Exploration

Minoo Mirsaeedi, Morteza Saheb Zamani – *Amirkabir U. of Technology, Iran*

12B.6 Scalable Neural-Network Stream Processor

P. Saeedi, A. Naghdinezhad, H. Esmaeilzadeh, S. Mohammadi, S. M. Fakhraie – *University of Tehran, Iran*

12B.7 Optimization of the Data Width to the Booked Quality of the Dobeshies-Wavelet Transform

Hahanova Irina, Barannik Vladimir, Litvinova Eugenia, Pobezhenko Irina – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

Third Day: September 10th, 2007 (Monday)

12B.8 A Design Method of Single Event Upset Tolerant Phase Locked Loop

Vazgen Melikyan, Aristakes Hovsepyan, Alik Sargsyan, Grigor Harutyunyan, Rafayel Ghasabyan – *Synopsys Armenia CJSC*

12B.9 Design of Reduced Quantum Cost Reversible BCD Adder

M. Mohamadi, M. Eshghi, A. Kaivani – *Shahid Beheshti U., Iran*

12B10 An Ultrawideband CMOS Low Noise Amplifier Design and Architectures Comparison

Rafayel Ghasabyan, Anahit Ghasabyan, Davit Badalyan, Artur Antonyan – *Synopsys Armenia CJSC*

Short Papers

9B.4 Design of a Low Power Digital Core for a Dual Mode UHF EPC RFID Tag

Vahid Roostaie, Vali Najafi – *KavoshCom R&D Group, Iran*
 Siamak Mohammadi – *University of Tehran, Iran*
 Ali Fotowat-Ahmady – *KavoshCom R&D Group, Iran*

Third Day: September 10th, 2007 (Monday)

12B11 Using Asynchronous Serial Transmission in Physical Design for Congestion Reduction
Ali Jahanian, Morteza Saheb Zamani – *Amirkabir U. of Technology, Iran*

16:00–16:30 **Session 13: Posters - Coffee Break**

17. Moore FSM Synthesis with Coding of Compatible Microoperations Fields

Alexander Barkalov, Larysa Titarenko, Alexander Barkalov, Jr. – *U. of Zielona Góra, Poland*

18. Fault Tolerant Implementation of SpaceWire Interface in SRAM-based FPGA

Supeng Chen and Lixin Yu – *Beijing Microelectronic Technology Inst., China*

19. Analysis of Output Resistance Bit-wise Control Method for Memory I/Os

William Movsisyan, Karen Sahakyan, Davit Shaghgamyán, Aristakes Hovsepyan, Davit Badalyan – *Synopsys Armenia CJSC*

20. Improving Behavioral Synthesis In Hardware/Software Co-Design

Mahmood Fazlali, Ali Zakerolhosseini, Mohammad K. Fallah, Sara Hashemi – *Shahid Beheshti U., Iran*

21. A Novel Fault-Tolerant Reconfigurable NoC Architecture

Mohammadreza Binesh Marvasti, Saeed Safari, Ali Afzali-Kusha, and Siamak Mohammadi

22. Optimal Thickness of Non-diffracting Subsurface Mirrors of X-Ray Optical Memory

Hakob (Akop) P. Bezirganyan – *Yerevan State U., Armenia*

Third Day: September 10th, 2007 (Monday)

<p>16:30–18:30</p> <p>Session 14A: Verification, Modeling, Education Moderator: Vyacheslav Kharchenko – <i>Nat. Aerospace U. "KhAI", Ukraine</i></p>	<p>16:30–18:30</p> <p>Session 14B: Algorithms Moderator: Sergey Mosin – <i>Vladimir State University, Russia</i></p>	<p>16:30–18:30</p> <p>Session 14C: Tutorial</p>
<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>14A.1 Optical Interconnects – Prospective Alternative for High-Speed Inter/Intra-Chip Galvanic Links Hovik V. Baghdasaryan – <i>State Engineering University of Armenia</i> Marian Marciniak – <i>Nat. Inst. of Telecommunications, Poland</i> Tamara M. Knyazyan – <i>State Engineering University of Armenia</i></p> <p>14A.2 Comparison of Commercial Parameter Extraction Tools for Spice SOI MOSFET Models Konstantin O. Petrosjanc, Lev M. Sambursky – <i>Moscow State Inst. of Electronics and Mathematics (Technical U.), Russia</i></p>	<p>Regular Papers</p> <hr style="border-top: 1px dashed black;"/> <p>14B.1 Numerical Approach for Distortion Analysis without High-order Derivatives in Device Models M.M.Gourary, S.G.Rusakov, S.L.Ulyanov, M.M.Zharov – <i>IPPM, RAS, Russia</i> K.K.Gullapalli, B.J.Mulvaney – <i>Freescale Semiconductor Inc., USA</i></p> <p>14B.2 3D Modeling of Different Layout SOI Mosfets under Physical Parameters Degradation Krupkina T. Y. – <i>Moscow Inst. of Electronic Engineering, Russia</i></p>	<p>Design for Yield and Reliability Yervant Zorian – <i>Virage Logic, USA</i></p>

Third Day: September 10th, 2007 (Monday)

14A.3 Modeling and Formal Verification of Hardware Designs

Niusha Hakimipour, Niloofar Razavi, Marjan Sirjani – *U. of Tehran, Iran*

14A.4 Towards Fast and Accurate Static Average-Case Performance Analysis of Embedded Systems: The MOQA Approach

Michel Schellekens, Rachit Agarwal – *U. College Cork, Ireland*
 Andrea Fedeli – *STMicroelectronics, Italy*
 Yiu Fai Lam – *Hong Kong Inst. of Science and Technology*
 Menouer Boubekour, Ka Lok Man, Emanuel Popovici – *U. College Cork, Ireland*

14B.3 Quasioptimal Algorithm of Timing Recovery in Autocorrelation Receiver of Phase Shift Keying Signal

Vitaliy A. Balashov – *Odessa Research Inst. of Communication, Ukraine*
 Victor V. Panteleev – *TELNET, Ltd., Ukraine*
 Leonid M. Lyakhovetsky – *Odessa Research Inst. of Communication, Ukraine*

14B.4 A new Approach to support Fault Simulation of Delay Insensitive Asynchronous Circuits with Synchronous Toolset

M. Mirzaaghatabar – *Sharif U. of Technology, Iran*
 A. Rasooli, B. Ghavami – *Amirkabir U. of Technology, Iran*
 Sh. Hessabi – *Sharif U. of Technology, Iran*

Third Day: September 10th, 2007 (Monday)

**14A.5 A Roadmap Towards
Microelectronics
Education in the Global
Era**

Andrzej Rucinski, Don Bouldin
– *U. of New Hampshire, USA*
Thaddeus Kochanski – *U. of
Tennessee, USA*

**14A.6 Graphical System Design
Technology Accelerating
the Modern Development
Cycle**

David Wilson, Aram Salatian –
National Instruments

Short Papers

**14A.7 Toward Embedded
Emotionally Intelligent
System**

M. R. Jamali, M. Valadbeigi, M.
Dehyadegari, Z. Navabi and C.
Lucas – *U. of Tehran, Shahid
Rajaei U., Iran*

**14B.5 Genetic Algorithms for
Fault Dictionary Size
Reduction**

D. Speranskiy, S. Mironov –
Saratov State U., Russia

Short Papers

**14B.6 An Algorithm for
Analysis of Analog Parts
of Circuits Described in
VHDL-AMS**

Arezoo Kamran, Amir Hossein
Jahangir – *Sharif U. of
Technology, Iran*

**14B.7 A Compact SOI/SOS
MOSFET Macromodel
Accounting for Radiation
Effects**

K. O. Petrosjanc, I. A.
Kharitonov, E. V. Orekhov, L.
M. Sambursky – *Moscow U. of
Electronics and Mathematics,
Russia*

Third Day: September 10th, 2007 (Monday)

14A.8 PeNCAD System – From Modeling to Synthesis of Concurrent Controllers

Agnieszka Węgrzyn, Marek Węgrzyn – *U. of Zielona Góra, Poland*

14A.9 A Software Tool for Generation of March Algorithms for Faults in SRAMs

G. Harutunyan – *Virage Logic, Armenia*

14A10 Model of Source Code Analyzer for Hardware Description Languages

Dmytro Melnyk, Sergei Zaychenko, Aleksandr Adamov, Vladimir Hahanov – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

14B.8 A Heuristic Method for Instruction-Set Extension Generation

Payman Loloeyan, Maghsoud Abbaspour – *Shahid Beheshti U., Iran*

14B.9 Transactional Data Analysis of Electronic System Level Models

Adamov A., Hahanov V., Melnik D., Chumachenko S., Hanko V. – *Kharkiv Nat. U. of Radio Electronics, Ukraine*

14B10 Detect Interfacial Cracks Based on Thermal Contact Resistance for Composite Materials

Chun-Yin Wu, Wen-Chang Lin – *Tatung U., Taiwan*

Third Day: September 10th, 2007 (Monday)

14A11 Processor Description in APDL for Design Space Exploration of Embedded Processors N. Honarmand, H. Sohofi – <i>U. of Tehran, Iran</i> M. Abbaspour – <i>Shahid Beheshti U., Iran</i> Z. Navabi – <i>U. of Tehran, Iran</i>	14B11 Diagnosis Method of Malicious Code in Executable Files Saprykin Aleksandr, Kiktenko Vitaly, Galagan Sergey, Kunitsky Artem – <i>Kharkiv Nat. U. of Radio Electronics, Ukraine</i>	
18:30–19:00	Session 15: Closing Session Yervant Zorian, Vladimir Hahanov	
20:00–22:00	Dinner: Restaurant (with Full Registration)	

Fourth Day: September 11th, 2007 (Tuesday)

Social Program: Optional Day Trip to Lake Sevan



SOCIAL PROGRAM

We hope that, regardless of the very tight time schedule, the symposium will create the opportunity not only for the exchange of scientific ideas but for some sightseeing as well.

September 7. Optional Tour to Khor Virap and Noravank.

The optional day tour includes a bus tour to the southern Armenia visiting beautiful monastery Khor Virap with close proximity and spectacular view to Mount Ararat. The tour continues to cross the larger agricultural area to the south well known with its grape yards, where a guided wine tour in Areni village will be organized (tasting wine, grapes and cheese), continued with a visit to Gladzor University Museum (a University from 13th century), Noravank Monastery (<http://en.wikipedia.org/wiki/Noravank>, a 13th century Armenian Apostolic Church Monastery) and a late lunch in a cave at Noravank canyon.

September 8. City Tour (Manuscript Museum, Cognac Factory, Tsitsernakaberd, Hayordats Toun).

City Tour including visit to Matenadaran (Manuscript museum), Tsitsernakaberd (Genocide museum), and Hayordats Toun – This tour will include a bus tour around the city exposing its beauty and welcoming the participants at one of the oldest cities in the world, 2700 years of age. The nowadays Yerevan however has all of the attributes of any modern European city with lots of very nice cafes, restaurants, fashionable shops and parks.

The city has a circular shape having the “Opera House Circle” in the very center from which different rays of streets and avenues head to different corners of the city. At the edges the city slowly turns in to squares forming the rural areas. The center is quite beautiful especially in the time of year the conference is being held at, with a lot of colors in the streets. The architecture of the center of the city is mostly 5 story-buildings made from beautiful red brick-stone. In the new constructed avenue, however one might find tall building made from concrete.

The visit would include, the Manuscript museum, where one can see lots of old writing and original Bible writing. The Genocide museum, Tsitsernakaberd, has also a special place in the tour which will take us away from the center up to one of the hills of the city on a



big plateau with beautiful sight of the city. During the tour we will also see the houses of Parliament, the Presidential white house and much more.

September 9. Visit to Etchmiadzin and surroundings.

Echmiadzin – is the holiest city in Armenia and the headquarters of the katholikos, the head of the Armenian Apostolic Church. It is in the Armavir province, about 20 km west of Yerevan. The main place of interest there is of course the holy church of Echmiadzin built in 301 AD, when Saint Grigor Lusavorich (Saint Gregory the Illuminator) pointed to the exact place on the land where it should be built.

September 10. Tour to Garni/Geghart (pagan temple and rock carved monastery).

Garni – Geghard – The pagan temple of Garni is a very nice temple in the region of which one can find facts of the so-long history of the Armenian Nation such as fortifications of the 3-rd millennium BC.

The church of Geghard is a unique architectural construction in the Kotayk province of Armenia, being partially carved out of the adjacent mountain, surrounded by cliffs. It is listed as a UNESCO World Heritage Site.

September 11. Optional Tour to Lake Sevan and Haghartsin.

The optional day tour including a visit to the largest lake in Armenia called Sevan, which is one of the largest high-altitude lakes in the world.

The tour continues to the north-eastern region of Armenia visiting beautiful monastery Haghartsin, that was built between 10th and 14th centuries under patronage of Bagratouni Dynasty of Armenian Kingdom.

The conference will offer a very rich and full social program at a full registration fee, however if You prefer to explore the city and/or country on your own please contact Tigran Atoyan at tigran.atoyan@viragelogic.com or directly during the conference and a tour of your choice will be organized.